

Code: EE5T6

**III B.Tech - I Semester – Regular/Supplementary Examinations
October 2018**

**LINEAR AND DIGITAL INTEGRATED CIRCUIT
APPLICATIONS
(ELECTRICAL & ELECTRONICS ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

PART – A

Answer *all* the questions. All questions carry equal marks

11 x 2 = 22 M

1. a) With an example explain the operation of difference amplifier.
- b) Derive gain in Non-Inverting amplifier.
- c) Explain the operation principle of sine wave generation.
- d) Draw the circuit diagram of 2nd order Low Pass Filter using Op-Amp?
- e) Mention the advantages of Switched capacitor filters.
- f) Draw the block diagram of PLL.
- g) Realize full subtractor using gates.
- h) Design a full adder circuit using 8X1 MUX.
- i) Write the differences between combinational and sequential circuits.
- j) What is race around condition?
- k) Compare latch and flip flop.

PART – B

Answer any *THREE* questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Draw the circuit diagram of differentiator by using IC 741 and explain its operation. 10 M
b) List out the ideal specifications of an op-amp. 6 M

3. a) Using a 741 op-amp design triangular /square waveform generator to have a output frequency of 1 kHz, a triangular output amplitude of $\pm 6V$ and a square wave output amplitude of approximately $\pm 10V$. 8 M
b) Design a second order low pass filter at cut off frequency of 1.2 kHz 8 M

4. a) Introduce PLL with its operating principles. 8 M
b) Explain internal block diagram and operation of 555 timer. 8 M

5. a) Draw the logic diagram of BCD to Decimal Decoder and explain its operation using truth table. 10 M
b) Design 4X16 Decoder using 2X4 Decoders. 6 M

6. a) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams. 8 M
- b) Explain the realization of SR flip-flop, JK flip-flop using D flip-flop. 8 M